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# LNA based on MEMS Capacitor and SPIRAL Inductor

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**ABSTRACT***:* In this study we designed a low noise amplifier based on cascode feedback topology was proposed for 2.5 GHz wireless application such as Bluetooth. We have used the MEMS capacitor and the SPIRAL Inductor in this design to get accurate outputs. The design was simulated with Cadence tool. The simulation result shows that the designed LNA achieves quite high quality.

**KEYWORDS***:* MEMS Capacitor, SPIRAL Inductor.

## I. INTRODUTION

Currently, due to its low cost and easy integration, CMOS is widely used to design wireless systems, especially in the radio frequency region. A low-noise amplifier (LNA) serves as the first building block of a wireless receiver.

The LNA amplifies the incoming wireless signal without adding much noise or distortion. The design of LNAs differs from that of an analog amplifier where voltage amplification is the goal. The design of LNAs is constrained by the maximum power transfer, i.e., maximally convert the received RF power to a voltage signal. Impedance matching is thus required at both the input and output port of a low-noise amplifier. In this paper, the design starts from a conventional cascode voltage amplifier. Input and output matching networks for maximum power transfer are then added at the input and output of the low-noise amplifier We will also see that low-amplifier might oscillate. Source and gate inductive degenerations are necessary for the LNA to operate stably. In addition to the maximum power transfer, the input impedance matching network can also be tuned so that the noise figure of the LNA is minimized. This is crucial for RF receivers as the noise figure of the LNA typically dominates the noise figure of the receiver.

In this paper, designed an low noise amplifier with carrier frequencie of 2.45 Ghz where we get the output of noise figure is 2db for power matching and 1.5 db for noise matching The noise performance of the LNA Dramatically influences the noise performance of the overall system [1]–[3].

Cascode amplifier is a two stage circuit consisting of a Trans conductance amplifier followed by a buffer amplifier. The word “cascode” was originated from the phrase “cascade to cathode”. This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher slew rate etc The reason behind the increase in bandwidth is the reduction of Miller effect. Cascode amplifier is generally constructed using FET (field effect transistor) or BJT ( bipolar junction transistor). One stage will be usually wired in common source/common emitter mode and the other stage will be wired in common base/ common emitter mode In this section, we first introduce a simple cascode voltage amplifier with a LC-tank load, The LC tank is composed of an ideal inductor in series with a resistor, and an parallel capacitor. The

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component values are annotated in the figure. The input of the amplifier is a 10 mV sinusoid at 2.45 GHz. The upper FET Q2 in the circuit is not affected by the Miller effect because the charging and discharging of the drain to source stray capacitance is carried out through the drain resistor and the load and the frequency response if affected only for high frequencies. Next, we replace the inductor-resistor with an spiral inductor and the ideal capacitor with an MEMS capacitor ,the inductors and capacitors have substrate connections

The radio frequency micro electromechanical system (RF MEMS) acronym refers to electronic components of which moving sub-millimetre-sized parts provide RF functionality. RF functionality can be implemented using a variety of RF technologies. Besides RF MEMS technology, III-V compound semiconductor (GaAs, GaN, InP, InSb), ferrite, ferroelectric, silicon-based semiconductor (RF CMOS, SiC and SiGe), and vacuum tube technology are available to the RF designer. Each of the RF technologies offers a distinct trade-off between cost, frequency, gain, large-scale integration, lifetime, linearity, noise figure, packaging, power handling, power consumption, reliability, ruggedness, size, supply voltage, switching time and weight.

An RF MEMs (micro electromechanical system) variable capacitor has been demonstrated with a 22:1 tuning range, tuning from 1.5 to 33.2 pF of capacitance. This capacitor was constructed using bistable MEMs membrane capacitors with individual tuning ranges of 70:1 to 100:1, control voltages in the 30–55 V range, switching speeds less than 10 mS, and operating frequencies as high as 40 GHz. These devices may eventually provide a variable alternative to electronic capacitors with improved tuning range and lower loss [4].

Si IC spiral inductors and transformers are analyzed using electromagnetic analysis. With appropriate approximations, the calculations are reduced to electrostatic and magneto static calculations. The important effects of substrate loss are included in the analysis. Classic circuit analysis and network analysis techniques are used to derive twoport parameters from the circuits. From two-port measurements, low-order frequencyindependent lumped circuits are used to model the physical behavior over a broadfrequency range. The analysis is applied to traditional square and polygon inductors and transformer structures, as well as to multi-layer metal structures. A custom CAD tool *ASITIC* is described, used for the analysis, design, and optimization of these structures.

Measurements taken over a frequency range from 100 MHz to 5 GHz show good agreement with theory [5] .In this paper in section II see,existing method and proposed method see in section III, and simulation outputs are in section IV. Finally, some conclusions of this paper are discussed and shared in Section V.

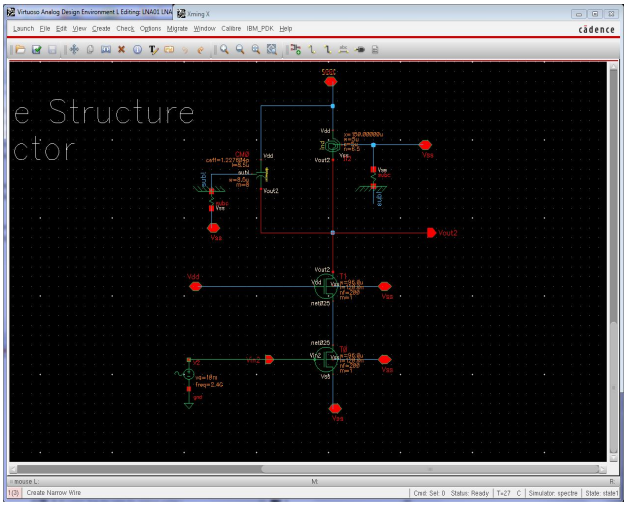


Fig1 : cascade amplifier with mems capacitor and spiral inductor

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## II. EXISTING METHOD

A 5 GHz low-noise amplifier (LNA) with a differential structure designed using 0.18 RFCMOS technology. An input balun is embedded into the LNA to enhance the gain, minimize the noise figure (NF), and miniaturize the overall chip size. By removing the passive input balun, the noise figure decreases and the gain is enhanced. Additionally, the entire chip size is reduced with the removal of the bulky input balun. To verify the feasibility of the proposed structure, we designed a 5 GHz low-noise amplifier (LNA) with a differential structure using 0.18 RFCMOS technology. The measured results show that the gain and noise figure of the proposed LNA are improved compared to those of a typical LNA The NF is minimized because the loss induced by the passive balun is removed. The first stage of the designed LNA performs the activities of the input balun and serves as the gain tage. To verify the feasibility of the proposed input-balun-embedded amplifier, we designed a typical LNA and the proposed LNA. We obtained a 29.4 dB gain with a NF of 1.85 dB. The measured dc power consumption is approximately 27 mW. The chip size is 1.0*0.74 $mm^2$ . From the measured results of the typical and proposed LNAs, we successfully prove the feasibility of the proposed method to minimize the NF and enhance the gain. In general, the input and output of a LNA are designed using a single-ended structure because the output of the antenna, which is connected to the input of the LNA, is a single-ended structure. However, if a single-ended LNA is designed using RFCMOS technology, gain reduction problems induced by the inductance of the bonding wires arise. In particular, the inductance of the bonding wire connected to the inductor for source degeneration in the first stage needs to be controlled to a high level of accuracy. Accordingly, a differential structure is popular in integrated circuits using CMOS technology. The differential structure can solve the problems described above. However, for LNAs, the passive balun essential n the differential structure degrades the noise performance because the loss induced by the input passive balun directly influences the overall noise figure. In this work, we propose an input-balun-embedded LNA structure to enhance the NF of the amplifier. Additionally, the chip size is reduced because the bulky passive input balun is removed. However, differential LNAs require input and output baluns, Thus, if the losses of the input and output re considered r a differential structure, the noise factor, , of the LNA can be described as follows:

$NF_{D=}1+(L_{IN}- 1) +–NF_{LNA} -1 /L^{-1}{}_{IN} + L_{OUT}-1/GDL^{-1}{}_{IN} = L_{IN}(N F_{LNA} +(L_{OUT}-1)/G_D)$

We designed a conventional LNA for a fair comparison of the performance levels of the proposed and the typical structure. The designed second stages for the typical and proposed amplifier are identical for a fair comparison[6] An output transformer acts as the load in the second stage and as the output balun. The supply voltage of the second stage enters through the primary part of the output transformer. The input and output transformers are designed using a spiral-type structure. The transformers are designed using a top metal layer, which is implemented using aluminum with a thickness of 2.34- . In this LNA, we use a supply voltage of 1.8 V. the size of the proposed LNA is reduced compared to that of the typical LNA due to the removal of the bulky input balun. We summarize the measured results of various LNAs in Table Ithe size of the proposed LNA is reduced compared to that of the typical LNA due to the removal of the bulky input balun. We summarize the measured results of various LNAs in Table IThe amount of improvement in the gain is affected by the loss of the input balun of the typical LNA and the increased input impedance of the proposed LNA. Ideally, the input impedance of the proposed LNA is two times higher than that of the typical LNA given that the size of the transistor connected to the input node of the proposed LNA is reduced
to half that of the typical LNA. Themeasured noise figure (NF) at 5 GHz is 1.85 dB,

## III. PROPOSED METHOD

**Maximum-Power-Gain Output Impedance Matching**

The power gain of an electrical network is the ratio of an output power to an input power. Unlike other signal gains, such as voltage and current gain, "power gain" may be ambiguous as the meaning of terms "input power" and "output power" is not always clear.The operating power gain of a two-port network, $G_P$, is defined as:

$$G_P = \frac{P_{\text{load}}}{P_{\text{input}}}$$

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where

- $P_{load}$ is the maximum time averaged power delivered to the load, where the maximization is over the load impedance, i.e., we desire the load impedance which maximizes the time averaged power delivered to the load.
- $P_{input}$ is the time averaged power entering the network

If the time averaged input power depends on the load impedance, one must take the maximum of the ratio--not just the maximum of the numerator.Three important power gains are operating power gain, transducer power gain and available power gain. Note that all these definitions of power gains employ the use of average (as oppose of instantaneous) power quantities and therefore the term "average" is often suppressed, which can be confusing at occasions.In this section, we convert the voltage-mode cascode amplifier studied earlier to a low-noise amplifier. The first step is to replace the input small-signal voltage source with an input port.The input port is needed for measuring a number of key parameters of the LNA including input impedance. Also, we add an output port at the output node. The output port is needed for measuring the output impedance of the cascode stage .In order to measure the output impedance of the cascode stage, we open up an ADE (Analog Design Environment) interface and choose the sp (S-parameter) analysis from the menu, as shown in Run the simulation and the results can be found in Results { Direct Plot { Main Form menu. In many cases, the parameter of Z22 can be approximated as the output impedance and in this design we use Z22 to denote the output impedance Zout, and Z11 to denote the input impedance Zin. Plot the output impedance values (real part and imaginary part for Z22) and record the values.Now, we can construct an output impedance matching network to convert the measured Z22 to 50 . The impedance matching process is done using Agilent ADS Smith Chart utilities. . By using the trial-and-error approach on the inductor turns (n) and capacitor multiplicity (m), the resulted matching can be close to the ideal matching network. This is verified by the output return loss S22 The output impedance looking into the matching network from the output port is for its real part and for its imaginary part respectively. We see that the output impedance looking into the output matching network is indeed close to a 50 resistor In telecommunications return loss is the loss of power in the signal returned or reflected by a discontinuity in a transmission line or optical fiber. This discontinuity can be a mismatch with the terminating load or with a device inserted in the line. It is usually expressed as a ratio in decibels (dB);

$$RL(\mathrm{dB}) = 10\log_{10}\frac{P_\mathrm{i}}{P_\mathrm{r}}$$

Where $RL$(dB) is the return loss in dB, $P_\mathrm{i}$ is the incident power and $P_\mathrm{r}$ is the reflected power.
Return loss is related to both standing wave ratio (SWR) and reflection coefficient (Γ). Increasing return loss corresponds to lower SWR. Return loss is a measure of how well devices or lines are matched. A match is good if the return loss is high. A high return loss is desirable and results in a lower insertion loss.return loss is used in modern practice in preference to SWR because it has better resolution for small values of reflected wave.

**Stability Analysis and Source/Gate Degeneration :**
Stability analysis of systems allows us to determine whether or not a system is stable or will be stable if perturbed. This is important in a wide range of applications since many behaviours observed in the real world can be described using differential equations. A low-noise amplifier could oscillate when its parasitic form a positive feed-
back loop. The unconditional stability criteria of LNAs are:
1. K > 1 and;
2. |Δ|< 1;
In control theory, and especially stability theory, a stability criterion establishes when a system is stable. A number of stability criteria are in common use. Stability may also be determined by means of root locus analysis.

Unconditional stability refers to a network that can "see" any possible impedance on the Smith chart from the center to the perimeter (up to gamma=1.0) at any phase angle. Gamma < 1 means that the real part of the impedance is positive. Note that any network can oscillate if it sees a real impedance that is negative, so if your system goes outside the normal Smith chart all bets on stability are off. In order to find out whether the LNA designed earlier and is stable or not, we plot its K value. The K value can be obtained from sp (S-parameter) analysis . It is seen that K > 1

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**Maximum-Power Gain Input Impedance Matching**

The input impedance of an electrical network is the equivalent impedance "seen" by a power source connected to that network. If the source provides known voltage and current, such impedance can be calculated using Ohm's Law. The input impedance is the Thévenin's equivalent circuit of the electrical network, modelled by an RL (resistor-inductor) or an RC (resistor-capacitor) combination, with equivalent values that would result in the same response as that of the network. It is also called $Z_{11}$ in terms of Z-parameters. Generally speaking, the exact definition depends on the particular field of study.

Generally in audio and hi-fi systems, amplifiers have an input impedance several orders of magnitude higher than the output impedance of the source device connected to that input. This concept is also called voltage bridging or impedance bridging. In this case,

$$Z_{load} >> Z_{source}$$

*The input impedance of the driven stage (load) is much larger than the output impedance of the driver stage (source).*

In general, this configuration will be more resistant to noise (particularly mains hum). Also the loading effects on the driving amplifier stage are reduced. In certain circuits a voltage follower stage is used to match the source and load impedance, which results in maximum power transfer.The procedures for maximum-power-gain input impedance matching is identical to the procedures for output impedance matchingWe briefly summarize the procedures : (1) measure $Z_{11}$ looking into the gate degeneration inductor; (2) design LC matching network transforming $Z_{11}$ to 50 .Since we have already done the maximum-power output impedance matching in Section. so at this moment, the input and output terminals are both matched to 50 external ports respectively. The resulted power gains are transducer power gain ($G_T$ ), available power gain ($G_A$) and operating power gain ($G_P$ ) where the three gains coincide at the same point at 2.4 GHz. Noise figure (NF) and noise factor (*F*) are measures of degradation of the signal-to-noise ratio (SNR), caused by components in a radio frequency (RF) signal chain. It is a number by which the performance of an amplifier or a radio receiver can be specified, with lower values indicating better performance.But, so far, we have not discussed another important issue in LNA design, noise. Spectre provides a convenient Noise Figure (NF) calculation menu, The noise figure at 2.45GHz is approximately 2 dB, which meets the specifications of most modern wireless applications including Bluetooth.

## IV. SIMULATION RESULTS

The proposed method has been implemented in cadence tool, in this tool we can produces software and hardware for designing integrated circuits, systems on chip(or, SoCs) and printed circuit boards.The outputs in this tool can be comparable that we can get the two or more outputs in a single window like $G_{T,}$(TRANSDUCER GAIN ) , $G_P$(POWER GAIN) ,$G_A$(AVAILABLE POWER GAIN).

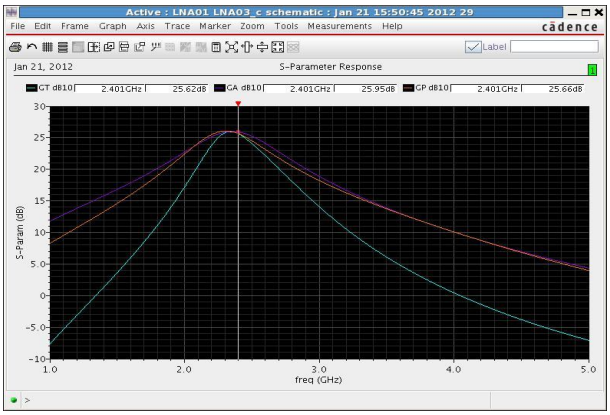


Fig 2: Transducer gain: $G_T$ ; Available power gain: $G_A$; Power gain: $G_P$

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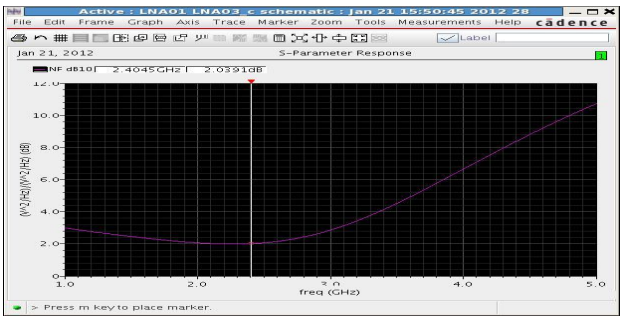


Fig 3 : noise figure of maximum power gain input impedence

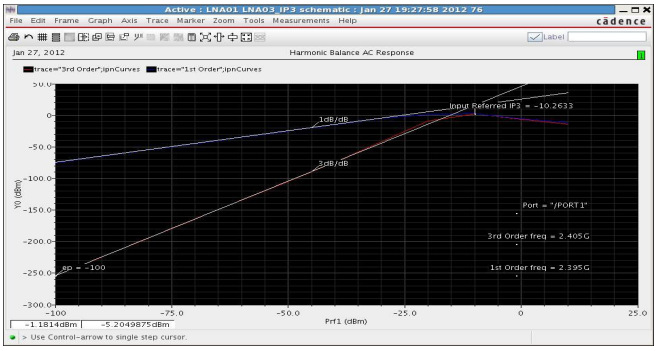


Fig 4 : IIP3 of the Low noise amplifier

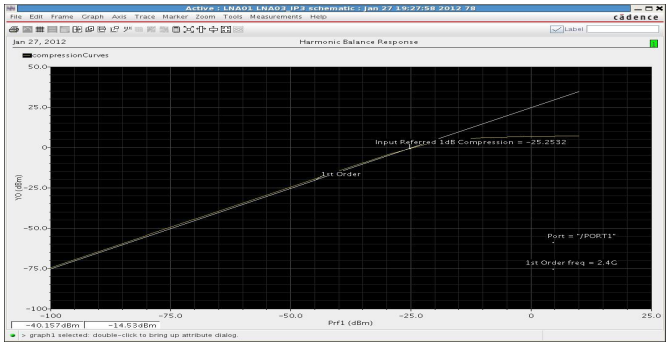


Fig 5 : 1dB compression point for the Low noise amplifier

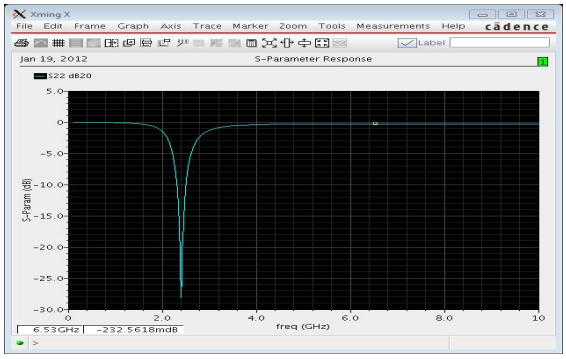


Fig 6: Output return loss S22 of cascode amplifier

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| REFERENCE | GAIN(db) | NOISE FREQUENCY(db) | IIP3 / 1P3(db) |
|---|---|---|---|
| [6] | 33.2 | 1.85 | -9 / 21.8 |
| THIS WORK | 25.9 | 2.48 | -10 / 25.2 |

Table 1 : comparison of results between the existing method and proposed method

## V. CONCLUSION

In this paper, we proposed an low noise amplifier working at 2.45 ghz proposed in cadence tool ensures that the generated data path works as an wireless Bluetooth application as the Bluetooth woks at 2.45 ghz frequency

## VI. ACKNOWLEDGMENT

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[5]Analysis, Design, And Optimization Of Spiral Inductors And Transformers For Si RF ICs By Ali M. Niknejad Master of Philosophy in Engineering-Electrical Engineering and Computer Sciences University of California Professor Robert G. Meyer, Chair
[6] Input Balun Embedded Low-Noise Amplifier With a Differential StructureJaehyuk Yoon, *Student Member, IEEE,* and Changkun Park, *Member, IEEE*